## REMARKS

Claims 1-11, 13-21 and 23-59 are pending in the present case. Claims 1-11, 17-21, 23-52 and 58 are amended herein. Claims 12 and 22 are canceled herein. Applicant respectfully requests reconsideration in view of the above amendments to the present application, and the arguments set forth below. No new matter is added herein. Applicant respectfully thanks the Examiner for accepting the drawings filed on April 5, 2002.

### CLAIM REJECTIONS

35 USC 102 (Insenser Farre Reference)

Claims 1, 3-8, 11-22, 25-32, 35-41, and 51-57 are rejected under 35 USC 102(e) over US Patent No. 6,460,172 to Insenser Farre, et al., (hereinafter Insenser). Applicant has reviewed the reference cited and respectfully asserts that it does not teach or suggest the embodiments of the present invention recited in Claims 1, 3-8, 11-22, 25-32, 35-41, and 51-57 for the following rationale.

As Applicant understands the reference, Insenser teaches a microprocessor based mixed signal field programmable integrated device. Insenser, c. 1, ll. 1-12. However, Applicant finds no teaching therein directed towards a microcontroller having a non-volatile memory, as recited in independent Claims 1, 11, 17, 35, 37, 51, 52 and 58, and their respective dependent claims, and Applicant respectfully agrees with the Examiner that Insenser does not teach a ROM or erasable memory (OA at 10 ¶35). The teachings of Insenser thus differ from the embodiments of the present invention recited in independent Claims 1, 11, 17, 35, 37, 51, 52 and 58, and their respective dependent claims.

As amended herein, independent Claim 1 reads as shown below, with underlining added herein for emphasis.

> 1. A microcontroller circuit comprising:
> a bus;
> a microprocessor coupled to said bus;
> a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and
> a plurality of functionalities coupled to said bus, wherein said functionalities comprise:
> an interconnect;
> an analog functional block coupled to said interconnect; and
> a digital functional block coupled to said interconnect.

Independent Claims 11, 17, 35, 37, 51, 52 and 58 are amended herein after a similar fashion, to recite a microcontroller having a non-volatile memory.

Applicant respectfully asserts that a microcontroller as recited in independent Claims 1, 11, 17, 35, 37, 51, 52 and 58 and their respective dependent claims is sometimes referred to as a "computer on a chip" and has, on a single integrated circuit (IC) device, a processor and non-volatile memory, such as a ROM. Freedman, A., Computer Desktop Encyclopedia 9th, Osborne/McGraw-Hill, NY (1971) at pp. 172 & 606. Microcontrollers thus have advantages relating to efficiency, speed, cost, and versatility and are used in a wide variety of applications.

Applicant respectfully asserts that, since Insenser does not teach a non-volatile memory, the reference does not anticipate Claims 1, 11, 17, 35, 37, 51, 52 or 58, or their respective dependent claims. Further, Applicant notes that Insenser expressly states that is its object "to provide a user-programmable [IC] that would include over the same silicon die a) a set of programmable logic cells as the ones used in already reported FPGAs." Id. at c.1, ll. 63-66, underlining added for

emphasis. Applicant respectfully points out that (1) an FPGA (Field Programmable Gate Array) is not a microcontroller, and (2) in its express statement quoted above, Insenser implicitly states applicability to FPGAs, and not to microcontrollers, as claimed herein. Applicants respectfully further assert therefore that Insenser implicitly teaches away from the embodiments recited in Claims 1, 11, 17, 35, 37, 51, 52 and 58 and their respective dependent claims. Thus, Applicant respectfully asserts that Insenser does not suggest these embodiments.

35 USC 103 (Insenser/Furtek References)

Claims 2, 9-10, 23-24, 33-34 and 42-49 are rejected under 35 USC 103(a) over Insenser in view of US Patent No. 5,894,565 to Furtek, et al. (hereinafter Furtek). Applicant has reviewed the references cited and respectfully asserts that they do not teach or suggest embodiments of the present invention recited in Claims 2, 9-10, 23-24, 33-34 and 42-49 for the following rationale.

Claims 2 and 9-10 and Claims 23-24 and 33-34 respectively depend upon independent Claims 1 and 17, discussed above. Claims 43-49 depend upon independent Claim 42, which as amended herein reads as shown below, with underlining added for emphasis.

> 42. A microcontroller circuit, comprising:
> a plurality of programmable analog circuit blocks configured to provide at least one of a plurality of analog functions;
> a plurality of programmable digital circuit blocks configured to provide at least one of a plurality of mathematical functions;
> a routing matrix configured to couple a subset of said plurality of programmable analog circuit blocks to a first subset of said plurality of programmable digital circuit blocks, at least a first one of said programmable analog circuit blocks being coupled to at

least a first one of said programmable digital circuit blocks; and

a programmable non-volatile memory coupled to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

Like independent Claim 1 and the other claims discussed above, Claim 42 is amended herein to recite a microcontroller having a non-volatile memory. Applicant respectfully repeats the points raised above in discussing those claims and respectfully re-asserts that Insenser implicitly teaches away from embodiments recited herein relating to microcontrollers having non-volatile memory.

As Applicant understands the reference, Furtek teaches a FPGA with distributed random access memory (RAM). Furtek, c. 2, l. 59-c. 3, l. 54. Applicant notes that the reference states that it "relates to programmable multifunctional digital logic array [ICs] of the type known as [FPGAs], and in particular to improvements in the structure of the configurable logic cells of such FPGAs, ..." Id. at c. 1, ll. 5-17. However, Applicant finds no teaching therein directed towards a microcontroller, as recited in Claims 2, 9-10, 23-24, 33-34 and 42-49 herein.

Applicant respectfully points out again that (1) an FPGA is not a microcontroller, and (2) in its statement quoted above, Furtek expressly states applicability to FPGAs, and not to microcontrollers, as claimed herein. Applicants respectfully further assert therefore that Furtek expressly teaches away from the embodiments recited in Claims 2, 9-10, 23-24, 33-34 and 42-49.

Insenser and Furtek both teach away from the embodiments recited in Claims 2, 9-10, 23-24, 33-34 and 42-49. Applicant finds no teaching in Insenser that cures this defect of Furtek. Likewise, Applicant finds no teaching in Furtek that cures the defects of Insenser. Thus, Applicant respectfully asserts that these references, combined or standing alone, do not teach or suggest the embodiments recited in Claims 2, 9-10, 23-24, 33-34 and 42-49.

35 USC 102 (Furtek Reference)

Claim 50 is rejected under 35 USC 102(a) and (b) over Furtek. Applicant has reviewed the reference cited and respectfully asserts that it does not teach or suggest the embodiment of the present invention recited in Claim 50 for the following rationale.

As amended herein, Claim 50 reads as shown below, with underlining added for emphasis.

> 50. A programmable analog circuit in a microcontroller, comprising a matrix of n by m plurality of programmable analog circuit blocks, each coupled to an adjacent block and configured to provide at least one of a plurality of analog functions.

Like the claims discussed above, Claim 50 is amended herein to recite a microcontroller. Applicant respectfully repeats the points raised above in discussing those claims and respectfully re-asserts that Furtek does not teach, and in fact expressly teaches away from embodiments recited herein relating to microcontrollers.

Applicant respectfully points out again that (1) an FPGA is not a microcontroller, and (2) Furtek expressly states applicability to FPGAs, and not to

microcontrollers, as claimed herein. Applicants thus respectfully further assert that Furtek expressly teaches away from the embodiments recited in Claim 50. Therefore, Applicant respectfully asserts that Furtek does not teach or suggest the embodiment recited in Claim 50.

35 USC 103 (Gammal Reference)

Claims 58 and 59 are rejected under 35 USC 103(a) over Insenser in view of US Patent No. 5,754,826 to Gammal, et al. (hereinafter Gammal). Applicant has reviewed the references cited and respectfully asserts that they do not teach or suggest the embodiments of the present invention recited in Claims 58 and 59 for the following rationale.

Claim 59 depends upon independent Claim 58. As amended herein, Claim 58 reads as shown below, with underlining added for emphasis.

> 58. In a system disposed in an integrated circuit, said system comprising:
> a microcontroller comprising a non-volatile memory;
> a subsystem coupled to said microcontroller, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input;
> an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and
> a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:
> a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions
> b) selecting an interconnection state to effectuate an interconnection between said analog

functionalities and said digital functionalities corresponding to said function;

c) selecting said connnectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c).

Like the claims discussed above, Claim 58 is amended herein to recite a microcontroller having a non-volatile memory. Applicant respectfully repeats the points raised above in discussing those claims and respectfully re-asserts that Insenser implicitly teaches away from embodiments recited herein relating to microcontrollers.

As Applicant understands the reference, Gammal's teaching "relates to the computer aided design of [ICs], and more particularly to the design of an [IC] which (sic) is intended to be manufactured by a number of foundries employing different fabrication processes." Gammal, c. 1, ll. 1-10. However, Applicant finds no teaching therein directed towards a microcontroller, or a process for configuring a system having a microcontroller, as recited in Claims 58 and 59 herein.

Further, in expressly directing its teaching to CAD for ICs, Applicant respectfully asserts that Gammal teaches away from an embodiment recited in Claims 58 and 59 herein, which recite a microcontroller and a process for configuring a system having such a microcontroller.

Insenser and Gammal both teach away from the embodiments recited in Claims 58 and 59. Applicant finds no teaching in Insenser that cures this defect of Gammal. Likewise, Applicant finds no teaching in Gammal that cures the defects of

Insenser. Thus, Applicant respectfully asserts that the references, either combined or standing alone, do not teach or suggest the embodiments recited in Claims 58 and 59.

## CONCLUSION

By the rationale stated above, Applicant respectfully asserts that the references cited do not teach or suggest embodiments of the present invention as recited in Claims 1-11, 13-21 and 23-59, and that these claims are thus allowable under 35 U.S.C. 102(a) and (b) and 35 U.S.C. 103(a). Accordingly, Applicant respectfully request that the rejections thereunder be withdrawn and that Claims 1-11, 13-21 and 23-59 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

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